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Negative Voltage Analysis Model for Evaluation on Control IC Driving of MOSFET Application

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Summary: In power converter applications, MOSFETs are used as switches to control the value of current or voltage and the control ICs are used to drive and control the MOSFET turn on/off to achieve high-frequency switching. In general, the absolute maximum negative voltage rating of the driving pin at these control IC is not sufficient and the driving pin would be damaged by negative voltage which would be induced as MOSFET switching off. The main purpose of this paper is to use the analysis model to evaluate and find out the parameter of MOSFET which leads to the control IC damaged.

Keywords: Parameters of MOSFET, Control IC, Gate drive, Negative voltage.

1. Introduction

In many of switching power supply and DC/DC converter applications, the gate drive pin of the control IC would be damaged by the negative voltage over the maximum rating. The driving of the power MOSFET is related to the switching speed of the turn-on/off in the switching power supply design. It needs to be considered the characteristic of the MOSFET and the capability of the gate driver at the same time [1-5]. Due to the parasitic inductance of the MOSFET lead and PCB circuit trace, the reverse recovery time (T_{rr}) and the reverse recovery charge (Q_{rr}) of MOSFET's parameters could generate the negative voltage by high current deviation [6-8].

2. Implementation of Circuit

Among circuitry topologies for the switching power supply, LLC converter is usually chosen as the main DC/DC topology, shown as Fig. 1. The S_1 and S_2 are the high voltage MOSFETs of half bridge and configured to output the square wave voltage. The low voltage MOSFETs S_3 and S_4 are the power switches of the secondary side synchronous rectifier to minimize power loss.

2.1. Gate Resistor

The switching speed of the turn-on/off is related the parasitic capacitance of the MOSFET and gate driving circuit [9-11]. The basic driving circuit is shown as Fig. 2. The resistor R_{gs} is to make the gate-source voltage down to 0 V while the gate-source voltage is open. Therefore, we recommend placing 10 kΩ ~ 100 kΩ resistor for reducing malfunction of the switch. The resistors R_{g_ext} and R_g and the input capacitance would affect the switching speed and the switching loss. For external R_{g_ext} selection to reduce switching loss, the following equation is recommended for the setting of V_{gs} rise/fall time by 5-time constants:

$$t_{rise/fall} = 5 \times (R_{g\_ext} + R_g) \times C_{iss}, \quad (1)$$

where C_{iss} is the input capacitance. R_g is the internal gate resistor. R_{g_ext} is the external resistor to change the switching speed for efficiency or EMI optimization in the gate drive circuit. From Potens' experience, we choose: where C_{iss} is the input capacitance. R_g is the internal gate resistor. R_{g_ext} is the external resistor to change the switching speed for efficiency, thermal or EMI optimization in the gate drive circuit [12, 13]. From Potens' experience, we choose:

$$\frac{t_{period}}{t_{rise/fall}} \geq 50, \quad (2)$$

where t_{period} is the period (cycle duration). The relation of the period and the switching frequency f_s is:

$$t_{period} = \frac{1}{f_s} \quad (3)$$

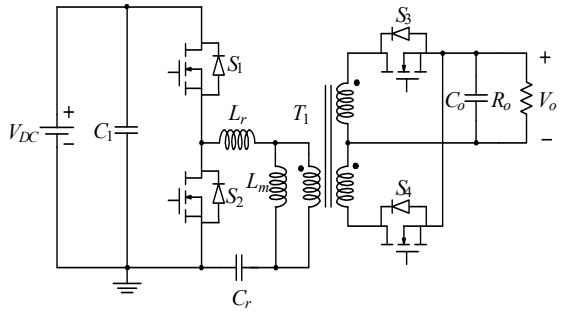

Fig. 1. The LLC converter for application.

From equation (1) to (3), R_{g_ext} can be expressed as below:

$$R_{g\_ext} \leq \frac{1}{250 \times f_s \times C_{iss}} - R_g, \quad (4)$$

We can use equation (4) to determine the suitable external resistor for the gate drive circuit.

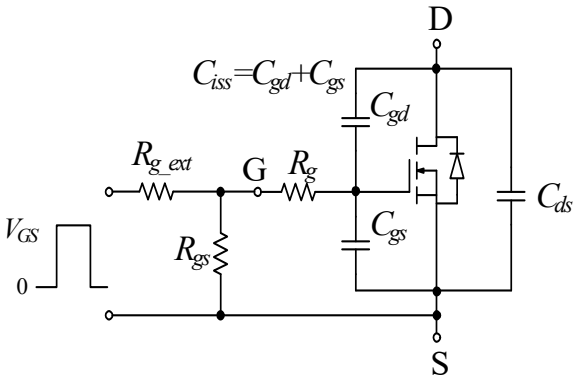

Fig. 2. The basic gate drive circuit.

2.2. Negative Voltage Analysis Model

The gate drive circuit loop with parasitic inductance (L_{p1}), the gate drive voltage (V_{GS}), the gate drive resistor (R_g), the gate drive resistor voltage (V_R), the gate drive current (I_g), and gate to source voltage (V_{gs}) are shown in Fig. 3.

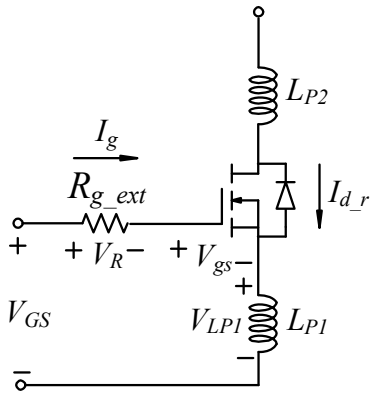

Fig. 3. The gate drive circuit with parasitic inductance.

In reverse recovery related period, I_{dr} is defined as the current of body diode. Fig. 4 is the relation between the reverse current of body diode and the voltage of parasitic inductance. The I_{RM} is the maximum reverse current of body diode, t_{rr_P} is the period of the positive induced voltage and t_{rr_N} is the period of the negative induced voltage. Therefore, the magnitude of the negative voltage can be derived as

$$V_{LP1} = L_{P1} \times \frac{dI_{d_r}}{dt} = \\ = L_{P1} \times \frac{0 - I_{RM}}{t_{rr\_N}} L_{P1} \times \frac{I_{RM}}{t_{rr\_N}} \quad (5)$$

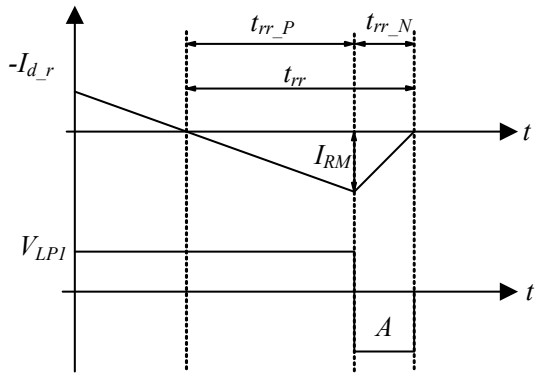

Fig. 4. Relation between the Id current and the voltage.

The relation of the reverse recovery charge, the reverse recovery time and the maximum reverse current is shown as

$$Q_{rr} = \frac{1}{2} I_{RM} \times t_{rr}, \quad (6)$$

The duration of the negative voltage means the energy stress on the gate drive pin of the control IC. The more duration the negative voltage sustains; the more control IC will be damaged. And we can drive the negative voltage energy as

$$A = |V_{LP1}| \times t_{rr\_N} \quad (7)$$

Substitute equation (5) and (6) into (7), we can derive the area of the negative voltage energy as

$$A = 2 \times L_{P1} \times \frac{Q_{rr}}{t_{rr}} \quad (8)$$

The equation (8) means that the energy might damage the IC is related to the ratio of the reverse recovery charge and the reverse recovery time.

From the above relation, we can establish the negative voltage analysis model considers the influence on the gate drive circuit and MOSFET equivalent circuit. The MOSFET parameters such as R_g, T_{rr} and Q_{rr} are as inputs of model and the parasitic parameters are assumed as another inputs of model. By this analysis model, we can obtain the negative voltage as the output and estimate the influence of the negative voltage on the gate drive pin of the control IC from this model. Fig. 5 is the negative voltage analysis model. In gate drive circuit, the gate drive voltage can be derived as

$$V_{GS} = V_{L_{P1}} + V_R + V_{gs} = \\ = L_{P1} \times \frac{dI_{d\_r}}{dt} + V_{gs} + I_g \times R_g \quad (9)$$

When the gate drive resistor is increased, the magnitude of the negative voltage is decrease as the following relationship:

$$R_g \uparrow \Rightarrow |V_{GS}| \downarrow \quad (10)$$

From above relation, the smaller the negative voltage is, the smaller the energy is. Therefore, the possibility for IC damaged is being low.

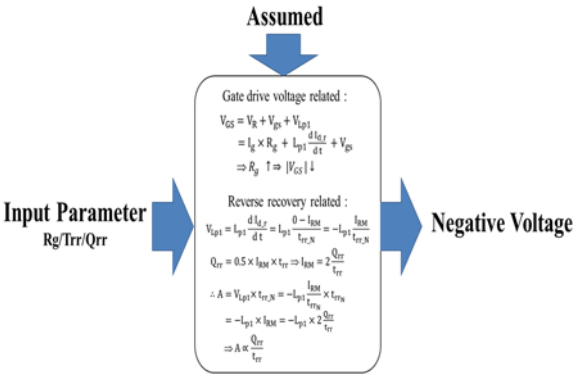

Fig. 5. Negative voltage analysis model.

3. Verification Based on Experimental Result

To demonstrate the effectiveness of the proposed, a 300 W LLC converter platform is chosen for demonstration. The operation principle of the proposed approach is experimentally implemented and verified through LLC converter platform utilizing secondary side synchronous rectifier. Fig. 6 is the prototype of LLC converter with driving, feedback circuit. The main component selection and circuit parameters are given in Table 1 [14].

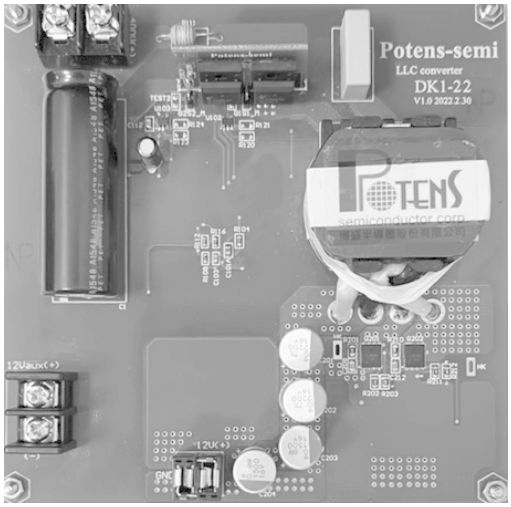

Fig. 6. Proposed circuit board.

Fig. 7 shows the turn on waveforms of the PDEC69F0BX-5 that Rg is 96 Ω, and Fig. 8 shows the turn on waveforms of the PDC6988BX-5 that Rg is 0.9 Ω. The result shows that a larger Rg will have a smaller negative voltage [15, 16]. We take three different MOSFETs as example. The measurement data of these three MOSFETs and the calculation results are shown in Table 1. From the Table 2, we could conclude that the result 3 with ratio of the reverse recovery charge and the reverse recovery time is the highest possibility to damage the gate drive pin of the control IC.

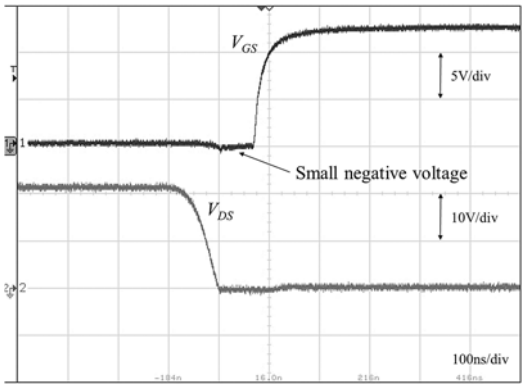

Fig. 7. The turn on waveforms of PDEC69F0BX-5.

Table 1. Parameters of main circuit.

Parameter	Value	Description
C_1	220 uF	450 V electrolytic capacitor
S_1, S_2	PJF14N65N	650 V, 14 A, SJ MOSFET
T_1	L_m = 600 μH, L_r = 100 μH	CC33, N_p: N_{s1}: N_{s2} = 34:2:2
C_r	68 nF	1 kV film capacitor
S_3, S_4	PDEC69F0BX-5/ PDC6988X-5	60 V MOSFET
C_o	1500 uF × 4	16 V electrolytic capacitor

Table 2. MOSFET parameters and negative voltage.

No.	t_{rr} (ns)	Q_{rr} (nC)	I_{RM} (A)	t_{rr_N} (ns)	V_{Lp1} (V)	$A=\lvert V_{Lp1} \times t_{rr\_N}\rvert$ (V·ns)	$\frac{Q_{rr}}{t_{rr}}$
Result 1	229.6	1946	16.95	40.45	-4.19	169.5	8.5
Result 2	244.1	2139	17.52	58.2	-3.01	175.2	8.8
Result 3	254.9	2300	18.05	50.3	-3.58	180.1	9

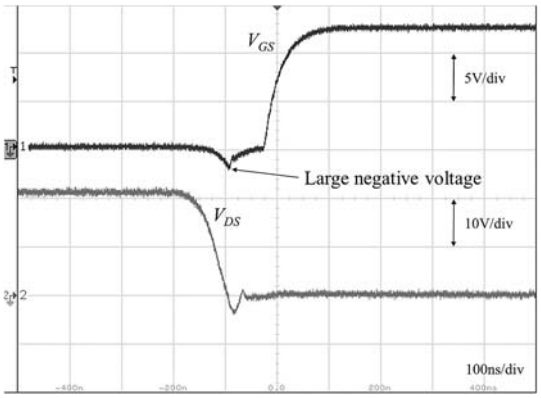

Fig. 8. The turn on waveforms of PDC6988BX-5.

4. Conclusions

This paper shows an analysis method to evaluate the influence of the negative voltage caused by the parasitic inductance of the MOSFET lead and PCB circuit trace and to impact on the drive pin of the control IC. The reverse recovery time is also the

highest possibility to damage the gate drive pin of the control IC. The more duration the negative voltage sustains, the more possibility that the control IC will be damaged. However, we could reduce the negative voltage drop at the gate drive pin by increasing the gate drive resistor.

References

[1]. STMicroelectronics, AN2626: MOSFET Body Diode Recovery Mechanism in a Phase-Shifted ZVS Full Bridge DC/DC Converter, Application Note, *STMicroelectronics*, 2007.

[2]. AN_201609_PL52_031: Benefits of Low Side MOSFET Drivers in SMPS, Application Note, *Infineon Technologies*, 2016.

[3]. M. Miura-Mattausch, S. Ooshiro, M. Suetake, Circuit simulation models for coming MOSFET generations, in *Proceedings of the International Conference on Simulation Semiconductor Processes and Devices*, 2000, pp. 106-111.

[4]. W. S. Choi, S. M. Young, D. W. Kim, Analysis of MOSFET failure modes in LLC, in *Proceedings of the 31st International Telecommunications Energy Conference (INTELEC'09)*, 2009.

[5]. C. D. G. Vladimir, T. J. Manuel, B. B. Hector, Z. T. Erwin, Q. M. Felix, L. A. M. Fernanda, Modeling and simulation of a MOSFET transistor in Verilog-A considering parasite elements, in *Proceedings of the IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA'15)*, 2015, pp. 1-5.

[6]. J. Victory, S. Pearson, S. Benczkowski, T. Sarkar, H. Jang, M. B. Yazdi, K. Mao, A physically based scalable SPICE model for shielded-gate trench power MOSFETs, in *Proceedings of the 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD'16)*, 2016, pp. 219-222.

[7]. P. Hower, C. Kaya, S. Pendharkar, C. Jones, Reverse-recovery safe operating area of diodes in power integrated circuits, in *Proceedings of the 24th International Symposium on Power Semiconductor Devices and ICs*, 2012, pp. 65-68.

[8]. R. Bonyadi, O. Alatise, J. Hu, J. A. Ortiz-Gonzalez, L. Ran, P. A. Mawby, Compact electro-thermal reliability modelling and experimental characterisation of bipolar latch up in SiC and CoolMOS power MOSFETs, *IEEE Trans. Power Electron*., Vol. 30, Issue 12, Jan. 2015, pp. 6978-6992.

[9]. V. Dimitrov, P. Goranov, D. Hvarchilkov, An analytical approach to model the switching losses of a power MOSFET, in *Proceedings of the 2IEEE International Power Electronics and Motion Control Conference (PEMC'16)*, 2016, pp. 928-933.

[10]. T. Lopez, E. Alarcon, Power MOSFET technology roadmap toward high power density voltage regulators for next-generation computer processors, *IEEE Trans. Power Electron*., Vol. 27, Issue 4, Apr. 2012, pp. 2193-2203.

[11]. B. Nguyen, X. Zhang, A. Ferencz, T. Takken, R. Senger, P. Coteus, Power MOSFET technology roadmap toward high power density voltage regulators for next-generation computer processors, *IEEE Trans. Power Electron*., Vol. 27, Issue 4, Apr. 2012, pp. 2193-2203.

[12]. Y. C. Son, K. Y. Jang, B. S. Suh, Integrated MOSFET inverter module for low-power drive system, *IEEE Trans. Ind. Appl*., Vol. 44, Issue 3, Apr. 2008, pp. 878-886.

[13]. X. Yu, P. Yeaman, Temperature-related MOSFET power loss modeling and optimization for DC-DC converter, in *Proceedings of the Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC'13)*, 2013, pp. 2788-2792.

[14]. PJF14N65N Datasheet, Potens, Hsinchu County, Taiwan, https://potens-semi.com/upload/product/PJF14N65N.pdf

[15]. PDEC69F0BX-5 Datasheet, Potens, Hsinchu County, Taiwan, https://potens-semi.com/upload/product/PDEC69F0BX-5.pdf

[16]. PDC6988X-5 Datasheet, Potens, Hsinchu County, Taiwan, https://potens-semi.com/upload/product/PDC6988X-5.pdf